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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/562,685	07/24/2006	Christian Val	4590-474	3796

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LOWE HAUPTMAN & BERNER, LLP
1700 DIAGONAL ROAD, SUITE 300
ALEXANDRIA, VA 22314

EXAMINER	
WHALEN, DANIEL B	
ART UNIT	PAPER NUMBER
2829	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/562,685	VAL ET AL.	
	Examiner	Art Unit	
	DANIEL WHALEN	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *14-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-7,12,13,17 and 18* is/are rejected.

7)☒ Claim(s) *2,3 and 8-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Claims 14-16 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected claims, there being no allowable generic or linking claim. Applicant's election **without** traverse of claims 1-13, 17, and 18 in the reply filed on 10/28/2008 is acknowledged.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. **Claims 1, 4, and 6-7** are rejected under 35 U.S.C. 102(b) as being anticipated by Fillion et al. (US 5,497,033; hereinafter "Fillion").

2. **Regarding Claim 1**, Fillion teaches a method for the interconnection of active components and passive components provided with terminals for their interconnection, comprising the steps of:

positioning and fixing the active (item 20) and passive (item 14) components on a flat support (item 10), the terminals (item 15) being in contact with the support (fig. 1a; col. 4, line 59—col. 5, line 11),

depositing a polymer layer (item 24) on all of the support and the components (fig. 1.b; col. 5, line 48- col. 6, line 3),

removing the support (fig. 1c & 2c; col. 6, line 30-41),

redistributing the terminals between the components and/or toward the periphery by means of metal conductors (item 32) arranged in a predetermined layout, to obtain a reconstituted heterogeneous structure (fig. 1.d-e; col. 8, line 7-27),

thinning the structure the polymer layer and at least one passive component by nonselective surface treatment (fig. 1.a-e and fig. 8.a-b; col. 12, line 29-63).

Regarding Claim 4, Fillion teaches that the surface treatment is carried out by nonselectively lapping and polishing (mechanical grinding) the polymer layer and the components (fig. 8.a-b; col. 12, line 29-63).

Regarding Claim 6, Fillion teaches that said redistributing of the terminals step comprises depositing a photo-etchable insulating layer (item 29), etching said layer in a pattern corresponding to the positioning of the terminals, depositing a metal layer (item 32) and etching said metal layer according to the predetermined layout of the metal conductors (fig. 1.e; col. 8, line 13-28).

Regarding Claim 7, Fillion teaches comprising a prior step of thinning the passive components (fig. 8.a-b; col. 12, line 29-53).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 5, 12, and 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fillion as applied to claims 1 and 14 above, and further in view of Nakamura et al. (US Pub 2002/0151103 A1; hereinafter "Nakamura").

5. **Regarding Claim 5**, Fillion teaches that the support includes an adhesive film (item 12a) and the removal step (fig. 2.a-b; col. 8, line 29-46). However, Fillion does not specifically disclose the details of removal step. Nakamura discloses that the removal is carried out by peeling the film (page 7, paragraph 141). Therefore, it would have been obvious to one of the ordinary skill in the art at the time of the invention to integrate the method of Fillion with peeling as taught by Nakamura as it is common technique for removing the adhesive material.

Regarding Claim 12, the combined teaching teaches the active and passive components being arranged on the support in order to form a set of identical patterns, furthermore comprising cutting (item 16, dicing from fig. 12 of Nakamura) the thinned heterogeneous structure around said patterns, to obtain a corresponding number of identical thinned heterogeneous elementary components (fig. 11-12 and fig. 14a-b).

Note that It is known to one of the ordinary skill in the art that for integrated circuit module fabrication, a set of identical components (dies) are produced and diced to obtain a corresponding number of identical components.

Regarding Claim 17, Fillion teaches a method for the three-dimensional interconnection of active and passive components provided with terminals for their interconnection, comprising:

positioning and fixing, on a plane support (10), at least one passive component (14) and a first active component (20), the terminals (15) being in contact with the support, and a terminal adapter (108), said adapter having metal contacts on two faces which are connected to each other, one of the faces being in contact with said support and the other face lying on the other side (fig. 4c-e),

stacking and bonding a second active component on said first active component (fig. 8d-e; col. 13, line 41-59),

depositing a polymer layer (item 24) on all of the support and said components (fig. 1.b; col. 5, line 48- col. 6, line 3),

removing the support (fig. 1.c; col. 6, line 30-41),

redistributing the terminals between the components and/or toward the periphery by means of metal conductors (item 32), making it possible to obtain a reconstituted heterogeneous structure (fig. 1.d-e; col. 8, line 7-27),

thinning said structure the polymer layer and the passive components by nonselective surface treatment (fig. 1.a-e and fig. 8.a-b; col. 12, line 29-63).

However, Fillion does not disclose that the terminals of said second component being on the opposite face from that in contact with the first component; and forming connections by connecting wires between the terminals of the second component and the contacts of the adapter. Nakamura teaches that the terminals of said second

component being on the opposite face from that in contact with the first component (fig. 6b); and forming connections by connecting wires (item 4) between the terminals of the second component and the contacts of the adapter (item 3c) (page 4, paragraph 88-91). Therefore, it would have been obvious to one of the ordinary skill in the art at the time of the invention to integrate the method of Fillion with a limitation discussed above as taught by Nakamura as it is common technique for wire-bonding process.

6. **Claim 13** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fillion and Nakamura as applied to claim 12 above, and further in view of Admitted Prior Art (Fig. 5; page 11, line 35 - page 12, line 5). Teaching of Fillion and Nakamura has been discussed above, However, the combined teaching does not disclose a method for the three-dimensional interconnection of active and passive components provided with terminals for their interconnection, comprising the steps of: producing thinned heterogeneous elementary components by the method as claimed in claim 12, the terminals being redistributed in particular toward the periphery, stacking and bonding the heterogeneous components, coating the stack with the aid of a polymer material, cutting the material to form, around said stack, a parallelepipedal block whose faces will expose the peripheral contacts of the active and passive components, depositing a metallization layer on at least a part of the faces, forming an interconnection network of the conductors by laser etching the metallization layer on the faces of the block. Admitted Prior Art (APA) teaches disclose a method for the three-dimensional interconnection of active and passive components provided with terminals for their

interconnection, comprising the steps of: producing thinned heterogeneous elementary components by the method as claimed in claim 12, the terminals being redistributed in particular toward the periphery, stacking and bonding the heterogeneous components, coating the stack with the aid of a polymer material, cutting the material to form, around said stack, a parallelepipedal block whose faces will expose the peripheral contacts of the active and passive components, depositing a metallization layer on at least a part of the faces, forming an interconnection network of the conductors by laser etching the metallization layer on the faces of the block. Therefore, it would be obvious to one of the ordinary skill in the art at the time of the invention to integrate the method of Fillion and Nakamura with a further method discussed above by APA so as to form three-dimensional heterogeneous interconnection.

7. **Claim 8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fillion as applied to claim 1 above, and further in view of Hirano et al. (US Pub 2003/0222335 A1; hereinafter "Hirano"). Teaching of Fillion has been discussed above. However, although Fillion discloses that the passive component can be capacitor (col. 5, line 12-27), Fillion does not disclose that the passive component is a ceramic capacitor with a zone of even and odd interdigitated electrodes, two ceramic filling zones on either side of the electrode zone and two lateral end terminals to which the even and odd electrodes are respectively connected, the prior thinning step consists in thinning one of said ceramic zones in a plane parallel to the electrodes. Hirano discloses that the passive component is a ceramic capacitor with a zone of even and odd interdigitated electrodes

(item 19), two ceramic filling zones (item 14) on either side of the electrode zone and two lateral end terminals (item 12) to which the even and odd electrodes are respectively connected, the prior thinning step consists in thinning one of said ceramic zones in a plane parallel to the electrodes (fig. 3A-3E; page 8, paragraph 87-94). Therefore, it would have been obvious to one of the ordinary skill in the art at the time of the invention to integrate the method of Fillion with a ceramic capacitor as taught by Hirano so as to improve the mounting characteristics.

8. **Claim 18** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fillion and Nakamura as applied to claims 17 above, and further in view of Oka et al. (US 6,441,495 B1; hereinafter "Oka"). Teaching of Fillion and Nakamura has been discussed above including the terminals of said second component being on the opposite face from that in contact with the first (lower) component (page 4, paragraph 88-91). However, the combined teaching does not disclose stacking and bonding at least one other active component on said second active component, forming connections by connecting wires between the terminals of each further component and the contacts of the adapter or the terminals of the lower component. Oka discloses stacking and bonding at least one other active component (item 2R) on said second active component (facing the same direction), forming connections by connecting wires (W) between the terminals of each further component and the contacts of the adapter or the terminals of the lower component (fig. 1; col. 1; line 10-24; col. 5, line 57-67). Oka Therefore, it would have been obvious to one of the ordinary skill in the art at the time of

the invention to integrate the method of Fillion and Nakamura with a limitation discussed above as taught by Oka so as to increase the mounting density of the semiconductor devices.

Allowable Subject Matter

9. **Claims 2, 3, 8-11** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

10. Applicant's arguments filed 08/13/2008 regarding claims 1 and 17 have been fully considered but they are not persuasive.

With respect to the argument that Fillion fails thinning a passive component with the polymer layer, Examiner respectfully traverses applicant's argument since Fillion clearly discloses thinning the passive component with the polymer layer (col. 12, lines 35-36, "part way through the chip").

With respect to the argument that Fillion fails to disclose removing the support, Examiner respectfully traverses applicant's argument since Fillion clearly disclose removing the support (see fig. 2a wherein the adhesive layer 12a and film layer 12b are removed).

11. With respect to the argument Applicant's arguments filed on 08/13/2008, see page 8, 1st paragraph and page 10, 2nd paragraph regarding claims 2, 3, and 8 have

been fully considered and are persuasive. Previous rejection of claims 2, 3, and 8 therefore have been withdrawn.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL WHALEN whose telephone number is (571)270-3418. The examiner can normally be reached on Monday-Friday, 7:30am to 5:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/D. W./
Examiner, Art Unit 2829
01/15/2009

Daniel Whalen
/Michael S. Lebentritt/

Primary Examiner, Art Unit 2829